IN THE ABSTRACT

Please amend the abstract as indicated below:

Abstract

~~" The invention concerns a~~ A clock recovery method in digital signal sampling~~,~~ wherein the clock ~~being~~ is generated from a phase-locking loop or PLL which multiples a given frequency by a whole number. ~~Said~~ The method ~~comprises a step which consists in~~ includes comparing the relative position of the signals with respect to the clock so as to determine whether a selected type of the clock transitions is in phase with the same type of signal transitions by: producing over a clock period several zones, one zone corresponding to the selected type of transitions; analysing the signal transitions relatively to the clock uplink or downlink transitions; cumulating in the corresponding zone the analysis results; determining on the basis of the accumulation whether the sampling clock frequency and/or phase needs to be modified or not. The invention is applicable to signals derived from graphics cards.